Amendments to the Specification:

Please amend the Title of the Application, as follows:

--METHOD FOR FORMING A CHANNEL ZONE OF A TRANSISTOR AND ~~PMOS~~ NMOS TRANSISTOR--

Please replace the paragraphs extending from page 1, line 8 - page 2 line 9, with the following paragraphs:

--The invention is concerned generally with the formation of a channel zone below a polysilicon layer of a transistor. In particular, the invention relates to a method for setting a desired doping profile in a p-type well zone of a ~~PMOS~~ NMOS field-effect transistor cell, and to a method for limiting the channel width of such a ~~PMOS~~ NMOS transistor cell.

A p-type well zone with reduced p-type doping is advantageous for depletion-mode ~~PMOS~~ NMOS field-effect transistor cells. During the traditional fabrication thereof, an additional mask is used therefor. The p-type well zone is traditionally formed by an implantation of boron and subsequent diffusion, thereby achieving the desired doping in the channel zone of the ~~PMOS~~ NMOS field-effect transistor. In order then to achieve the desired reduced p-type doping, conventionally holes or pillars are formed in the mask, thus resulting in a more lightly p-doped well zone in the cell (cf. U.S. Patent No. 5,736,445 and German patent DE 19 526 183 C1). If only the gate electrode is perforated with holes, the channel zone remains highly doped

and so a p^--type layer cannot take effect in the p-type well zone.

Accordingly, the desire that arises here is to enable a ~~PMOS~~ NMOS transistor cell with a p-type well zone having reduced p-type doping, without an additional mask, in order to produce a more lightly doped p-type well in a ~~PMOS~~ NMOS field-effect transistor cell, for example in a *coolMOS*™ MOSFET cell (cool-MOS™ is a trademark of Infineon Technologies AG).--

Please replace the paragraph beginning on page 7, line 21, with the following paragraph:

--In a first embodiment, the method according to the invention provides the following steps in the formation of the channel zone of a ~~PMOS~~ NMOS field-effect transistor: --

Please replace the paragraph beginning on page 9, line 9, with the following paragraph:

--In accordance with a second embodiment, the method according to the invention serves for the channel width shading of integrated ~~PMOS~~ NMOS transistor cells and is distinguished by the following steps:--

Please replace the paragraph beginning on page 10, line 1, with the following paragraph:

--In an alternative embodiment, the method according to the invention serves for the channel width shading of an integrated ~~PMOS~~ NMOS transistor cell and is distinguished by the following steps: --

Please replace the paragraph beginning on page 10, line 11, with the following paragraph:

--~~A PMOS~~ An NMOS transistor cell fabricated by this method is distinguished by the fact that the transistor cell has slots or webs in sections of the polysilicon layer lying above the channel zone, the slots being introduced such that they connect the channel zones of adjacent transistor cells and the webs being composed of polysilicon, lying within the polysilicon hole delimiting the source region, and being short-circuited with the source electrode.--

Please replace the paragraph beginning on page 10, line 20, with the following paragraph:

--The afore-mentioned ~~PMOS~~ NMOS transistor cell according to the invention is particularly preferably a vertical depletion-mode MOSFET transistor cell, e.g. a coolMOS™-FET transistor cell.--

Please replace the paragraph beginning on page 11, line 4, with the following paragraph:

--Although the invention is illustrated and described herein as embodied in a method for forming a channel zone of a transistor and ~~PMOS~~ NMOS transistor, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.--

Please replace the paragraphs on page 11, lines 19 - 25, with the following paragraphs:

--Figs. 1A and 1B are diagrammatic cross sections through a section of ~~a PMOS~~ an NMOS-FET transistor cell, illustrating two successive steps of the method according to the invention for forming a more lightly doped channel zone;

Fig. 1C is a perspective illustration of the section of ~~a PMOS~~ an NMOS-FET cell in accordance with Fig. 1B;--

Please replace the paragraphs on page 13, lines 14 - 24, with the following paragraphs:

--It should be noted that, while the exemplary embodiments described below relate to a vertical ~~PMOS~~ NMOS transistor or vertical ~~PMOS~~ NMOS transistor cells, the method according to the invention can also advantageously be applied to lateral

MOS transistors and also to bipolar transistors such as, for example, IGBTs and normal MOS transistors.

Referring now to the figures of the drawing in detail and first, particularly, to Figs. 1A to 1C thereof, there is shown a first embodiment of a method according to the invention for forming a channel zone of ~~a PMOS~~ an NMOS field-effect transistor.--

Please replace the paragraph beginning on page 14, line 1, with the following paragraph:

--Firstly, in accordance with Fig. 1A, holes 2 are formed in the gate region and bars 1 are formed in the source region in a polysilicon layer 11. The holes 2 and the bars 1 reach the plane of an n-type epitaxial layer 10, in which a p-type well defining a p-type channel is intended to be formed. The holes 2 in the gate region 8 and the bars 1 in the source region 7 serve as a mask for a doping step illustrated with reference to Fig. 1B. At least one of the parameters form, spacing, number and diameter in each case of the holes 2 and of the bars 1 is critical for the doping profile of the p-type channel zone that is established after the diffusion in accordance with Fig. 1B. In accordance with Fig. 1B, which shows the state of the field-effect transistor cell after the diffusion, the section 12A (body) in the source region 7 is p^+-

doped and extends deeper into the n-type epitaxial layer 10 than the section 12b of the p-type channel zone in the gate region 8, where the section 12b of the p-type channel zone is p^--doped. In the p^--type region 12b, an n^--type depletion-mode implantation can then be effected in order to form a gate electrode 14 for a depletion-mode FET by means of a masked or whole-area ~~AS~~ As or P implantation. A source electrode 13 can then be implanted in a customary manner in the source region.--

Please replace the paragraph beginning on page 15, line 18, with the following paragraph:

--Furthermore, a method for channel width shading in the case of an exemplary vertical ~~PMOS~~ NMOS transistor is described with reference to Figs. 2A, 2B to 6, which is implemented by means of slots 20 (Figs. 2A, 2B and 3) in the polysilicon 11 or by means of webs 22 made of polysilicon 11 within the poly-hole 13 (Figs. 4 to 6).--

Please replace the paragraph beginning on page 15, line 25, with the following paragraph:

--The method according to the invention for channel width shading aims to appreciably increase the resistance of the channel or of the lead on a proportion of the channel width. In accordance with Figs. 2A, 2B and 3, the corresponding

channel regions of adjacent cells are connected to one another by means of a p-doped region. By virtue of this connection, a continuous potential gradient does not occur in the p-doped region and the channel thus appears to have an infinite length in these regions. A restricted or shaded channel width can thus be utilized for charge carriers. Consequently, during the implantation for fabricating the channel regions, the p-type dopant (e.g. ~~AS~~ As or P) is also introduced into the slots 20, thereby connecting the actual channel regions of adjacent cells. The gate resistance could represent a problem in this method. The increase in the gate resistance can be counteracted by a gate ring. The variant shown in Fig. 2B differs from that in Fig. 2A in that the gate resistance is reduced to a lesser extent there. The variant shown in Fig. 3 differs from the embodiments of Figs. 2A and 2B in terms of the more favorable form of the slots 20, which curve partly around the hexagonal form of the poly-holes 13. Two slots 20 of this type are provided per poly-hole 13, for symmetry reasons, such that there is always only one slot 20 pointing toward the adjacent hexagonal poly-hole 13.--

Please replace the paragraphs on page 18, lines 7 - 23, with the following paragraphs:

--It should be noted that various experiments in the meantime indicate that the transconductance β of the transistor can

also be varied well by means of the lead resistance (~~AS~~ As implantations). This could mean, for example, providing p^{++} with a higher dose. However, this measure could have a very disadvantageous effect on the on resistance R_{on}.

The method according to the invention for the channel width shading of integrated ~~PMOS~~ NMOS transistor cells which has been described above and illustrated with reference to Figs. 2A, 2B to 6 has the advantage that an entire photolithography plane is obviated and that the gate capacitance of the transistor is heavily reduced. With these advantages, a coolMOS™ transistor improved by means of the method according to the invention can venture into market segments hitherto held to be unattainable. Similar advantages to those described above for vertical MOSFETs also apply to lateral MOSFETs and to IGBTs.--